

APPARATUS AND METHOD FOR RTL BASED FULL CHIP  
MODELING OF A PROGRAMMABLE LOGIC DEVICE

Abstract of the Disclosure

[0080] An RTL representation for a LAB is generated. A full chip RTL model is then generated using a plurality of the LAB RTLs. Using the full chip RTL model, a full chip  
5 simulation of the PLD chip is performed to verify and debug the electronic design.